Ref. 12588ROUS01U

**Title:** **Method and apparatus for transmitting arbitrary electrical signals over a data network**

## *Field of the Invention*

The present invention relates to the field of data transmission, such as data transmission that may occur in a data network that can be synchronous or asynchronous. More particularly, it pertains to a method and apparatus for transporting data signals of arbitrary transmission rate over a data network characterized by a range of allowable transmission rates.

## *Background of the Invention*

Evolution of the current data transport networks is hindered by a number of constraints. For example, the optical transport networks operate according to fiber specific transmission protocols, each having different levels of operation, administration, maintenance and provisioning (OAM&P) functionality, so that the nodes must be equipped with protocol-specific hardware and software. In addition, handling a plurality of protocols at speeds over 100 Mb/s poses real problems for the current generation of microprocessors.

One way to increase the speed (and bandwidth) of the network is to replace the electronics components with optical components. The increased transport capacity requirements are also met by the introduction of point to point optical

fiber systems, carrying TDM signals. An example of a TDM network is SONET/SDH, which transports hierarchically multiplexed lower rate tributaries into a higher rate TDM signal. SONET/SDH is a physical layer technology which is currently used as a transport service for ATM, SMDS, frame relay, T1, E1, etc. SONET/SDH provides the ability to combine and consolidate traffic from different locations through one facility (grooming) and reduces the amount of back-to-back multiplexing. More importantly, network providers can reduce the operation cost of their transmission network by using the comprehensive OAM&P features of SONET.

Originally, optical transport networks were intended to be bit-rate and data format independent, thus providing for the transportation of a wide variety of data signals. Unfortunately, current optical transport networks, including SONET/SDH networks, do not achieve this goal, as the line rates for these networks have been restricted to a set of discrete transmission rates. Similarly, current electrical transport networks, such as the DS3 electrical network, are also limited to particular, discrete transmission rates. Thus, data characterized by a transmission rate that does not belong to the set of pre-defined transmission rates is not directly transportable over such data networks. In many cases, a user signal must undergo a mapping operation to be able to be transported by the data network.

The mapping of one rate or format into another is well known. For example, Bellcore TR-0253 describes in detail the standard mappings of the common asynchronous transmission formats (DS0, DS1, DS2 and DS3, among others) into SONET. Similar mappings are defined for the ETSI hierarchy mapping into SDH.

Unfortunately, the standards or proprietary schemes allow the transportation of only a very specific set of signals, with format specific hardware. Thus, these methods of mapping cannot be used to map rates that vary significantly from the standard. Furthermore, these mappings are each precisely tuned for a particular format and a particular bit-rate, with for example a ±20ppm (parts per million of the bit rate) tolerance. If a signal has, for example, a bit rate even 1% different than that of a DS3, it cannot be transported over a SONET/SDH network. In addition, a different hardware unit is generally required to perform the mapping of each kind of signal.

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A' In a somewhat different approach discussed in the U.S. patent application serial No. 09/349,086 (Roberts), entitled "Mapping Arbitrary Signals into SONET", filed on July 8, 1999 and assigned to Nortel Networks Limited, arbitrary electrical signals are converted into SONET optical signals by using a synchronizer. The synchronizer maps the arbitrary electrical signals into SONET signals such that the electrical signals can be recovered with low timing jitter at low cost at the far end. This mapping method can be used for tributaries of almost any continuous format. The synchronizer recognizes selected protocols, frames on them, and effects the corresponding performance monitoring.

Also, U.S. patent application serial No. 09/438,516 (Roberts et al.), entitled "Detection of Previous Section Fail for a Transparent Tributary", filed on November 12, 1999 and assigned to Nortel Networks Limited, discloses a method and apparatus for transmitting a continuous digital signal of an arbitrary rate R1 over a synchronous network as a transparent tributary. The rate R1 of the continuous digital

signal is detected and a protocol corresponding to the rate R1 is determined, according to which protocol a set of performance parameters on the continuous digital signal are measured and reported.

The background information provided above indicates that there is a need in the industry to improve the technology for transparently transmitting electrical data signals, in particular signals of arbitrary transmission rate, over a data network.

***Summary of the Invention***

The present invention provides in a first broad aspect a synchronizer for mapping an electrical digital signal of arbitrary transmission rate for transport over a data network characterized by a range of allowable transmission rates. The data network can be an optical network or an electrical network. Also, the network may be a synchronous network or an asynchronous network. The synchronizer includes a data recovery unit, a clock generator unit and a mapping unit. The data recovery unit receives the electrical digital signal and recovers therefrom a stream of data bits and a first data clock signal indicative of the arbitrary transmission rate. The clock generator processes the first data clock signal for generating a second data clock signal indicative of a line transmission rate that falls within the range of allowable transmission rates for the data network. The mapping unit uses the first and the second data clock signals to map the stream of data bits into a frame for transmission over the data network.

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A4 According to a second broad aspect of the invention, there is provided a desynchronizer for reverse mapping a frame received over a data network into an electrical digital signal having an arbitrary transmission rate. The desynchronizer includes a clock recovery unit, a reverse mapping unit and a data transmitter unit. The clock recovery unit receives the frame and recovers therefrom a data clock signal indicative of a line transmission rate. The reverse mapping unit extracts from the frame a stream of data bits according to a reverse mapping algorithm, on the basis of the line transmission rate. The data transmitter unit transmits the extracted stream of data bits on a basis of the line and arbitrary transmission rates, for generating an electrical digital signal characterized by the arbitrary transmission rate.

Advantageously, the synchronizer/desynchronizer as described above renders the data network substantially bit-rate and data format independent, whether the data network is synchronous or asynchronous, electrical or optical. Thus, an electrical digital signal of arbitrary transmission rate, where this arbitrary transmission rate does not fall within the range of allowable transmission rates for the data network, may be transparently transported over the data network.

The present invention is further directed to a method for transmitting a digital signal of arbitrary transmission rate over a data network characterized by a range of allowable transmission rates.

## *Brief Description of the Drawings*

These and other features of the present invention will become apparent from the following detailed description considered in connection with the accompanying drawings. It is to be understood, however, that the drawings are provided for purposes of illustration only and not as a definition of the boundaries of the invention, for which reference should be made to the appending claims.

Figure 1 is a block diagram of a communication network with the mapping system according to an embodiment of the present invention;

Figure 2 is a functional block diagram of a synchronizer as shown in Figure 1;

Figure 3 is a functional block diagram of the mapping unit shown in Figure 2;

Figure 4 is a functional block diagram of a desynchronizer as shown in Figure 2.

## *Detailed Description*

Figure 1 illustrates a transmission system 100 in which data signals are transparently transported over an asynchronous data network 102, in accordance with a non-limiting example of implementation of the present invention. Only one direction of transmission, as shown by the arrows, is illustrated in this figure for purposes of clarification and simplification. The data network 102 may be optical or electrical, examples of the data network 102 including an asynchronous electrical DS3 or DS1 network, an early 622

Megabit/second asynchronous fiber network and a more recent asynchronous optical network based on OTN standards, among many other types of asynchronous data networks. Note that the use of a synchronous data network, such as a SONET/SDH network, instead of an asynchronous data network is still within the spirit of the invention. In all cases, the data network 102 is characterized by a range of allowable, discrete transmission rates.

In a specific example, the data network 102 is an asynchronous electrical DS3 network. An arbitrary electrical digital signal S is being transmitted from endpoint A to endpoint B, and is to be transported as a DS3 signal S' over the DS3 network 102. The signal S is characterized by an arbitrary transmission rate R, while the signal S' is characterized by a line transmission rate R'. The term "arbitrary" implies that the signal S can carry various types of services, such as voice, data and video, among others. A receiver 104 recovers the data bits for the respective continuous digital signal S. Specific to the present invention, endpoint A is provided with a synchronizer 106 for mapping the data bits of the signal S into a DS3 signal S'.

After the signal S is mapped into the DS3 signal S', the signal S' is launched by a DS3 transmitter 112 over the electrical DS3 network 102 towards the endpoint B.

The reverse operation is performed at endpoint B. More specifically, the DS3 receiver 114 recovers the data in signal S' and presents this data to a desynchronizer 118. The desynchronizer 118 re-arranges the recovered data bits according to the respective format associated with the signal S and transmits these bits with the appropriate arbitrary transmission rate R to a transmitter 120. The transmitter

120 launches the recovered signal S over an associated network or to a local client.

VNS A3

Figure 2 is a functional block diagram of the synchronizer 106 that receives an electrical digital signal S at input 200. The synchronizer 106 comprises a data recovery unit 202 that is operative to extract from the signal S a stream of data bits and a data clock signal, hereinafter referred to as the first data clock signal. This first data clock signal is indicative of the transmission rate R for the signal S. As shown in Figure 2, the data recovery unit 202 includes a receiver 212 and a flexible clock recovery circuit 214. The flexible clock recovery circuit 214 is capable of clock recovery over a broad continuous range of bit-rates. An example of such a circuit is disclosed in the Canadian patent application filed on November 10, 1999 and published on June 22, 2000, entitled "Apparatus and Method for Versatile Digital Communication", by Habel et al., assigned to Northern Telecom Limited.

The data recovery unit 202 passes the extracted first data clock signal to a clock generator unit 204. The clock generator 204 processes the first data clock signal received from the data recovery unit 202 for generating a new data clock signal indicative of a line transmission rate that falls within the range of allowable transmission rates for the electrical DS3 network 102, as will be discussed in further detail below. The new data clock signal generated by the clock generator unit 204 is hereinafter referred to as the second data clock signal.

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In a specific, non-limiting example of implementation, the clock generator unit 204 includes a multiplier 206 that implements frequency multiplication for generating the second

data clock signal, and an input 208 for receiving a control signal. In particular, the multiplier 206 is operative to multiply the first data clock signal up to a second data clock signal that is indicative of a transmission rate that is compatible with a line transmission rate of the network 102. The control signal received at input 208 is generated by a frequency control unit 210 that automatically controls the multiplier 206.

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A5 The automatic frequency control unit 210 is operative to detect the incoming arbitrary transmission rate for the signal and, on the basis of a pre-defined desired line transmission rate, automatically set the multiplier 206 such that the appropriate frequency multiplication is applied to the first data clock signal for increasing the latter to the second data clock signal. In an alternative, the frequency control unit 210 is itself controlled by a system operator and receives provisioning information, such as the desired line transmission rate, from the system operator. The well documented concept of frequency multiplication is well known to those skilled in the art and, as such, will not be described in further detail.

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A6 The second data clock signal is passed from the clock generator unit 204 to a mapping unit 206. The mapping unit 206 is responsible for mapping the stream of data bits into a DS3 frame for transmission over the asynchronous electrical DS3 network 102, on a basis of the second data clock signal. Thus, the mapping algorithm is independent of the format and bit rate of the network 102 in the sense that the line transmission rate is recovered from the first data clock signal of the incoming digital signal S. This is contrary to existing mapping systems in which the line transmission rate

is recovered from a local clock reference of the network 102.

As shown in Figure 3, the mapping unit 206 includes a transparent mapper 300 and a wrapper frame generation unit 302. The transparent mapper 300 receives as inputs the stream of data bits and the first data clock signal extracted from the electrical digital signal S by the data recovery unit 202, as well as the second data clock signal generated by the clock generator unit 204. The transparent mapper 300 is operative to map the extracted data bits into a DS3 frame, while the wrapper frame generation unit 302 is coupled to the transparent mapper 300 for generating a *wrapped* DS3 frame for transmission over the DS3 network 102, as will be discussed in further detail below.

In a specific, non-limiting example of implementation, the transparent mapper 300 maps the stream of data bits extracted from the electrical digital signal S into a DS3 frame with evenly interspersed fixed stuff bits and adaptive stuff bits, where the implemented mapping algorithm is in effect a stuffing algorithm. The transparent wrapper 300 divides the DS3 frame into evenly sized blocks, and determines the number of fixed stuff bits for each block. Since the rate R of the signal S is not known in advance, the number of variable stuff bits is determined on the go, based on a function $\beta$ which gives information about the phase difference between the arbitrary transmission rate R of the signal S and the line transmission rate that is generated by the clock generator unit 204.

The transparent mapper 300 comprises a flexible buffer 304 and a mapper 306. The buffer 304 generates $\beta$ during processing of the current block of the DS3 frame, and this $\beta$

is used for mapping of the next block. The value of β gives the position of the variable stuff bits and the number of the valid bits in the next block of the DS3 frame. Buffer 304 receives the bits of a block at the recovered first data clock signal and transmits the bits to the mapper 306 at the rate of a gapped clock. The gapped clock is derived from the second data clock signal generated by the clock generator unit 204 and is discontinued at appropriate phase instances. The discontinuities (gaps) are given by β and by the number of fixed stuff bits.

The value of β may change between adjacent blocks, as not all blocks have the same number of adaptive stuff bits, but β remains constant within each block.

The stuffing algorithm also defines the binary bit reversal of β, which is denoted α. That is, the most significant bit of β becomes the least significant bit of α; similarly the least significant bit of α becomes the most significant bit of β.

α is also determined on a per block basis, and as in the case of β, the value of α may change between the adjacent blocks but does not change within a block.

The adaptive algorithm also defines a counter C and a value D. C is the counter of bits in a block, and is represented by a 10 bit binary number. The counter C increments from 1 to 1023 and, as such, identifies the timeslot occupied by a bit in the block.

D is the bit-wise transition delta of C and is represented by a 10 bit binary number with exactly one bit set. This set bit is in the position of a 0 to 1 transition

that occurs when counter C advances with one bit. Using Boolean functions, each bit of D is given by the bits of range n and n-1 of counter C, according to the equation:

$$D_n = C_n \text{ AND NOT } (C-1)_n$$

In order to spread stuff bits more or less evenly among valid data in the block, the stuffing algorithm uses the following relationship:

Valid (C, $\beta$), if any bit of ($\alpha_{1,2...n}$ AND $D_{1,2...n}$) is non zero

where the mapper 306 defines a valid location, which is a location for a data bit, and an invalid location, which is a location for a stuff bit. On the basis of the valid and invalid locations of the stuffing algorithm, the mapper 306 provides an output signal, with the stuff bits (fixed and variable) distributed uniformly among the extracted data bits within a DS3 frame, to the wrapper frame generation unit 302.

For more information on the stuffing algorithm, the user can refer to the US patent application 09/348,087 by Kim B. Roberts, filed on July 8th 1999 and assigned to Nortel Networks Corporation. The contents of this application are incorporated herein by reference.

The wrapper frame generation unit 302 is responsible for generating a wrapped DS3 frame for transmission over the electrical DS3 network 102. In particular, DS3 overhead information is placed into the appropriate fixed stuff bit positions. A time slot interchange unit 308 re-arranges the overhead bits in the frame so that the DS3 equipment in the network 102 can recognize the DS3 frame, thus "wrapping" the DS3 frame. The wrapped DS3 frame is then transmitted towards the endpoint B over the network 102, via transmit equipment

310.

It is not deemed necessary to discuss the standard operation of the wrapper frame generation unit 302, including the addition of overhead information to the frame, in more detail because it is well known to those skilled in the art.

Figure 4 is a functional block diagram of a desynchronizer 118 that performs the reverse operation to that performed by the synchronizer 106, in a very similar manner, and is provided with similar functional blocks. In particular, the desynchronizer 118 receives a wrapped DS3 frame over the DS3 network 102 at input 400 and includes a clock recovery unit 402, a reverse mapping unit 404 and a data transmitter unit 406.

The clock recovery unit 402 includes receive equipment 408 operative to recover from the wrapped DS3 frame a stream of data bits in electrical format, as well as circuitry 410 for recovering from the wrapped DS3 frame a data clock signal indicative of the line transmission rate. In a specific example, a flexible clock recovery circuit 410, similar to the circuit 214 described above, is capable of clock recovery over a broad continuous range of bit-rates.

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A7 The data clock signal indicative of the line transmission rate and the stream of data bits, including stuff bits, are input to a reverse mapping unit 404. The reverse mapping unit 404 includes a time slot interchange unit 412 and a demultiplexer 414 for extracting the OCO and FEC information from the corresponding timeslots on a basis of the recovered data clock signal indicative of the line transmission rate. The reverse mapping unit 404 further includes a reverse mapper 416 for reverse mapping the stream

of data bits extracted from the wrapped DS3 frame, on a basis of the particular mapping algorithm implemented at the synchronizer 106.

In accordance with the non-limiting specific example of implementation given above for the mapping unit 206, the reverse mapper 416 reversibly maps the stream of data bits based on β and the recovered data clock signal indicative of the line transmission rate. The reversibly mapped stream of data bits is passed to a data transmitter unit 406.

The data transmitter unit 406 includes a buffer 418 for receiving the stream of data bits at the rate of a gapped clock, derived from the recovered data clock signal indicative of the line transmission rate. The data transmitter unit 406 extracts the stream of data bits from the buffer 418 at the arbitrary transmission rate, and transmits the generated electrical digital signal S characterized by the arbitrary transmission rate to a local client.

Depending on the user specifications, a conversion unit for converting the recovered signal S may also be provided at the endpoint B. For example, if the user is an optical access network, recovered signal S will be converted to an optical format.

Note that β, which is determined at the synchronizer 106 at endpoint A during the mapping operation, is communicated to the desynchronizer 118 at endpoint B for the reverse mapping operation, along with the data clock signal indicative of the arbitrary transmission rate for the signal S. More specifically, β and the data clock signal indicative of the arbitrary transmission rate of the signal S are

encoded into the overhead information of the signal S' for transmission from the synchronizer 106 to the desynchronizer 118.

The synchronizer 106 and the desynchronizer 118 discussed above can be implemented in hardware or in software. A software implementation requires a computing platform executing a program element. The computing platform includes a Central Processing Unit (CPU) that is coupled to a memory over a data bus. The memory holds the individual program entities that implement the various functional units of the synchronizer 106 or of the desynchronizer 118 and also data on which the program entities operate. The computing apparatus communicates with the external world through an Input/Output (I/O) hardware interface that connects with the data bus.

Note that in an alternative example of implementation, the above-described mapping system is used to transport a DS3 electrical signal S over a higher rate optical network 102. In this example, the transparent mapper 300 of the synchronizer 106 maps the signal S into a 2.5 Gigabit/second frame. The frame wrapper generation unit 302 of the synchronizer 106 adds Optical Channel Overhead (OCO) and Forward Error Correction (FEC) information to the frame, thus generating a wrapped frame S' for transmission over the optical network 102.

The above description of a preferred embodiment under the present invention should not be read in a limitative manner as refinements and variations are possible without departing from the spirit of the invention. The scope of the invention is defined in the appended claims and their equivalents.